Interfacing DDR & DDR2 SDRAM With Cyclone II Devices

August 2004, ver. 1.0 Application Note 361

Introduction

Over the years, as applications have become more demanding, systems have increasingly resorted to external memory as a way to boost performance while reducing cost. Single data rate (SDR) memories gave way to double data rate (DDR) memories as system designers continually sought solutions to boost system performance without increasing system complexity and cost.

DDR2 SDRAM is the next generation of DDR SDRAM technology, with improvements including lower power consumption, higher data bandwidth, enhanced signal quality, and on-die termination schemes. DDR2 SDRAM brings higher memory performance to a broad range of applications, such as PCs, embedded processor systems, image processing, storage, communications, and networking.

DDR SDRAM is currently the popular memory of choice. Designers looking to save system power are moving toward using DDR2 SDRAM, which uses a lower 1.8-V I/O voltage compared to the DDR SDRAM I/O voltage of 2.5 V. Table 1 shows the DDR and DDR2 SDRAM interface support in Cyclone™ II devices.

Table 1. DDR & DDR2 SDRAM Support in the Cyclone II Devices *Note (1)*

DDR Memory Type	I/O Standard	Maximum Clock Rate		
		-6 Speed Grade Commercial Wire-Bond	-7 Speed Grade Commercial Wire-Bond	-8 Speed Grade Commercial Wire-Bond
DDR SDRAM *(2)*	SSTL-2	167 MHz	167 MHz	133 MHz
DDR2 SDRAM *(2)*	SSTL-18	167 MHz	167 MHz	133 MHz

Notes to Table 1:
(1) These numbers are preliminary until Cyclone II characterization is final.
(2) Specifications are based on the use of clock control delay circuitry.

Cyclone II devices can interface with DDR and DDR2 SDRAM in device or module configurations up to 167 MHz and 333 megabits per second (Mbps). This application note describes the DDR and DDR2 SDRAM interfacing in Cyclone II devices and provides detailed timing analysis.

Use this application note together with the *External Memory Interfaces* chapter of the *Cyclone II Device Handbook*.

DDR & DDR2 Functional Description

This section provides information on DDR and DDR2 SDRAM.

DDR SDRAM

DDR SDRAM is a 2n prefetch architecture with two data transfers per clock cycle. In the 2n prefetch architecture, two data words are fetched from the memory array during a single read command. DDR SDRAM uses a strobe signal (DQS) that is associated with a group of data pins (DQ) for read and write operations. Both the DQS and DQ ports are bidirectional. Address ports are shared for write and read operations.

Write and read operations are sent in bursts, and DDR SDRAM supports burst lengths of two, four, and eight. This means that you need to provide 2, 4, or 8 groups of data for each write transaction, and you will receive two, four, or eight of data for each read transaction. The interval between the time the read command is clocked into the memory and the time the data is presented at the memory pins is called the column address strobe (CAS) latency. DDR SDRAM supports CAS latencies of 2, 2.5, and 3, depending on the operating frequency. Both the burst length and CAS latency are set in the DDR SDRAM mode register.

DDR SDRAM specifies the use of the SSTL-2 class II I/O standard termination. Each DDR SDRAM device is divided into four banks, and each bank has a fixed number of rows and columns and can hold between 64 Mb to 1 Gb of data. Only one row per bank can be accessed at one time. The ACTIVE command opens a row and the PRECHARGE command closes a row.

DDR2 SDRAM

DDR2 SDRAM is the second generation of the DDR SDRAM memory standard. DDR2 SDRAM is a 4n prefetch architecture with two data transfers per clock cycle. In the 4n prefetch architecture, four data words are fetched from the memory array during a single read command. DDR2 SDRAM uses a strobe signal (DQS) that is associated with a group of data pins (DQ) for read and write operations. Both the DQS and DQ ports are bidirectional. Address ports are shared for write and read operations.

Although DDR2 SDRAM devices can use the optional differential strobes (DQS and DQS#), Cyclone II devices do not support this mode. Cyclone II devices only use the DQS signal to read from and write to the DDR2 SDRAM device.

Write and read operations are sent in bursts, and DDR2 SDRAM supports burst lengths of four and eight. This means that you need to provide four or eight groups of data for each write transaction, and you will receive four or eight groups of data for each read transaction. The interval between the time the read command is clocked into the memory and the time the data is presented at the memory pins is called the column address strobe (CAS) latency. DDR2 SDRAM supports CAS latencies of three and four, depending on the operating frequency. DDR2 SDRAM does not support half-clock latencies. Both the burst length and CAS latency are set in the DDR2 SDRAM mode register.

Besides CAS latency, DDR2 SDRAM offers posted CAS additive latencies of zero, one, two, three and four. During the read operation, instead of getting the data CAS latency after the read command is issued, you can send the read command earlier with a particular additive latency value. The additive latency setting specifies how many clock cycles earlier you should send the read command.

The memory device holds the read command for the number of cycles specified by the additive latency. The read latency is the sum of the additive latency and the CAS latency. During the write operation, instead of sending the data one clock cycle after the write command is issued, you can send the write command earlier with a particular additive latency value. The additive latency setting specifies how many clock cycles earlier you send the write command. The memory device holds the write command for the number of cycles specified by the additive latency. The write latency is one clock cycle less than the read latency.

DDR2 SDRAM specifies the use of the SSTL-18 class II I/O standard termination and can hold between 64 Mb to 4 Gb of data. DDR2 SDRAM devices with capacities up to 512 Mb are divided into four banks, and devices with capacities between 1 and 4 Gb are divided into eight banks. Only one row per bank can be accessed at one time for devices with four banks. Only four banks can be accessed at one time for devices with eight banks. The ACTIVE command opens a row and the PRECHARGE command closes a row.

DDR2 SDRAM uses a delay-locked loop (DLL) inside the memory device to edge-align the DQ and DQS signals with respect to CK. The DLL in the memory devices is turned on for normal operation and is turned off for debugging purposes. All timing analyses done in this document assume that the DLL in the memory devices is on.

Since DDR2 SDRAM devices also have adjustable data-output drive strength, Altera recommends that you use the highest drive strength the memory device can support for maximum performance. DDR2 SDRAM devices also offer parallel on-die termination and the on-die termination has an effective resistance of either 75 or 150 Ω.

Differences Between DDR & DDR2 SDRAM

DDR2 SDRAM offers some key improvements over DDR SDRAM. DDR2 SDRAM has on-die termination to improve signal integrity and timing margin. DDR2 SDRAM has a feature called posted CAS additive latency, which improves the bus efficiency over the DDR SDRAM. DDR2 SDRAM consumes less power since it uses the SSTL-18 I/O standard termination instead of the SSTL-2 I/O standard termination that DDR SDRAM uses.

Interface Pins

Table 2 shows the DDR SDRAM interface pins and how to connect them to Cyclone II devices.

Table 2. DDR SDRAM Interface Pins

Pins	Description	Cyclone II Pin Utilization
DQ	Bidirectional read/write data	DQ
DQS	Bidirectional read/write data strobe	DQS
CK	System clock	User I/O pin
CK#	System clock	User I/O pin
DM	Optional write data mask, edge-aligned to DQ during write	DM
All other	Addresses and commands	User I/O pin

Table 3 shows the DDR2 SDRAM interface pins and how to connect them to Cyclone II devices.

Table 3. DDR2 SDRAM Interface Pins (Part 1 of 2)

Pins	Description	Cyclone II Pin Utilization
DQ	Bidirectional read/write data	DQ
DQS	Bidirectional read/write data strobe	DQS
DQS# *(1)*	Optional bidirectional differential read/write data strobe	N/A
CK	System clock	User I/O pin
CK#	System clock	User I/O pin

Table 3. DDR2 SDRAM Interface Pins (Part 2 of 2)		
Pins	**Description**	**Cyclone II Pin Utilization**
DM	Optional write data mask, edge-aligned to DQ during write	DM
All other	Addresses and commands	User I/O pin

Note to Table 3:
(1) The DQS# signal in DDR2 SDRAM devices is optional. Cyclone II devices do not use DQS# pins when interfacing with DDR2 SDRAM.

This section provides a description of the clock, control, address, and data signals on DDR and DDR2 SDRAM devices.

Clock, Strobes & Data

DDR and DDR2 SDRAM devices use the CK and CK# signals to clock commands and addresses into the memory. The memory also uses these clock signals to generate the DQS signal during a read via a DLL inside the memory. The skew between CK or CK# and the SDRAM-generated DQS signal is specified as t_{DQSCK} in the DDR and DDR2 SDRAM data sheet.

Both DQ and DQS signals are bidirectional (the same signals are used for both writes and reads). The DQS# pins in DDR2 SDRAM are not used in Cyclone II DDR2 SDRAM interface. A group of DQ pins is associated with one DQS pin.

In ×8 and ×16 DDR SDRAM devices, one DQS pin is associated with eight DQ pins. Cyclone II devices support both ×8 and ×16 DDR SDRAM. Use the DQS pins and their associated DQ pins listed in the Cyclone II pin tables when interfacing with DDR and DDR2 SDRAM from Cyclone II I/O banks.

Table 4 shows the number of DQS/DQ groups supported in Cyclone II devices.

Table 4. Cyclone II DQS & DQ Bus Mode Support (Part 1 of 2) Note (1)			
Device	**Package**	**Number of ×8 Groups**	**Number of ×16 Groups**
EP2C5	144-pin TQFP (2)	3	0
	208-pin PQFP	7 (3)	3

Table 4. Cyclone II DQS & DQ Bus Mode Support (Part 2 of 2) *Note (1)*

Device	Package	Number of ×8 Groups	Number of ×16 Groups
EP2C8	144-pin TQFP *(2)*	3	0
	208-pin PQFP	7 *(3)*	3
	256-pin Fineline BGA	8 *(3)*	4
EP2C20	256-pin FineLine BGA	8	4
	484-pin FineLine BGA	16 *(4)*	8
EP2C35	484-pin FineLine BGA	16 *(4)*	8
	672-pin FineLine BGA	20 *(4)*	8
EP2C50	484-pin FineLine BGA	16 *(4)*	8
	672-pin FineLine BGA	20 *(4)*	8
EP2C70	672-pin FineLine BGA	20 *(4)*	8
	896-pin FineLine BGA	20 *(4)*	8

Notes to Table 4.

(1) Numbers are preliminary until devices are available.

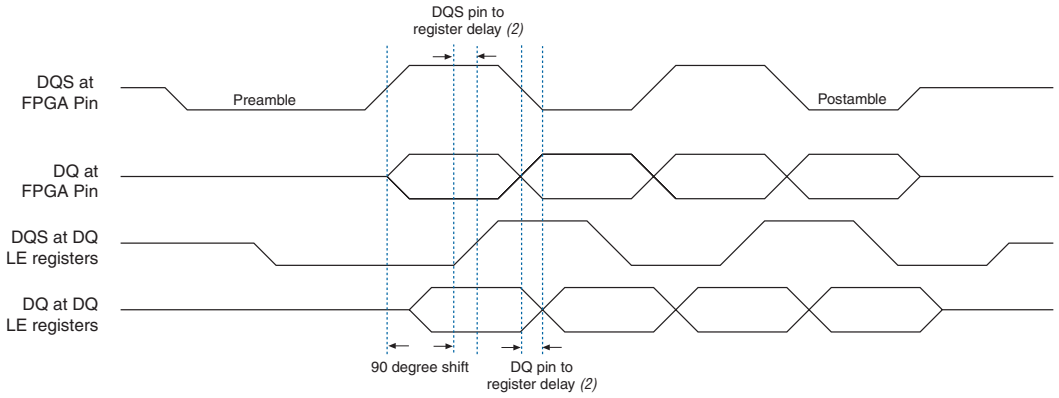
(2) EP2C5 and EP2C8 devices in the 144-pin TQFP package do not have any DQ pin groups in I/O bank 1.

(3) Because of available clock resources, only a total of 6 DQ/DQS groups can be implemented.

(4) Because of available clock resources, only a total of 14 DQ/DQS groups can be implemented.

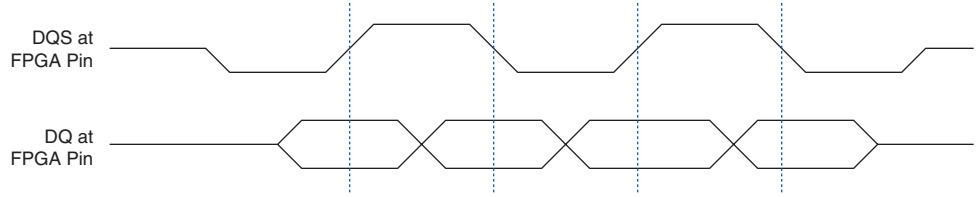
During a read from the memory, the data strobe signals (DQS) are edge-aligned with the data signals (DQ). During a write to the memory, the Cyclone II device transmits the DQS signals center-aligned relative to the DQ signals. Figures 1 and 2 illustrate the DQ and DQS relationships during a DDR and DDR2 SDRAM read and write. The memory controller on the device center-aligns the DQS signal during a write and shifts the DQS signal during a read so that the DQ and DQS signals are center-aligned at the capture register. The Cyclone II device uses a phase-locked loop (PLL) to center-align the DQS signal with respect to the DQ signals during writes and uses dedicated DQS programmable delay chain circuitry to shift the incoming DQS signal during reads.

Figure 1. DQ & DQS Relationship During DDR & DDR2 SDRAM Read in Burst of 4 Mode *Note (1)*



Notes to Figure 1:
(1) DDR SDRAM supports burst lengths of 2.
(2) The DQS and DQ pins to the register delay are not the same.

Figure 2. DQ & DQS Relationship During DDR & DDR2 SDRAM Write in Burst of 4 Mode *Note (1)*



Note to Figure 2:
(1) DDR SDRAM supports burst lengths of 2.

The setup (t_{DS}) and hold (t_{DH}) times for the DQ and data mask (DM) pins at the memory during a write are relative to the edges of DQS write signals and not the CK and CK# clocks. The memory setup and hold times are equal ($t_{DS} = t_{DH}$) and are typically 0.45 ns for a 167-MHz DDR SDRAM device. Unlike the DDR SDRAM devices, the DDR2 SDRAM memory setup and hold times are not necessarily equal depending on the input data slew rate and the usage of the differential DQS# signal. Since Cyclone II devices do not use the differential DQS# signal from the DDR2 SDRAM memory devices for clocking, t_{DS} is 0.15 ns and t_{DH} is 0.28 ns for 167-MHz DDR2 SDRAM devices. Refer to the DDR2 SDRAM data sheet for information on the memory's setup to hold time.

The DDR and DDR2 SDRAM t_{DQSS} timing is the amount of time between when the memory detects the write command to the first DQS transition. The DQS signal is normally generated on the positive edge of system clock to meet the t_{DQSS} requirement. The DQ and DM signals are clocked using a –90° shifted clock from the system clock. The edges of the DQS signal are centered on the DQ and DM signals when they arrive at the DDR SDRAM device.

To minimize the skew between the arrival times of these signals, the DQS, DQ, and DM board trace lengths should be similar.

The DDR and DDR2 SDRAM t_{DQSS} write requirement states that on writes, the positive edge of the DQS signal must be within ±25% (±90°) of the positive edge of the DDR and DDR2 SDRAM clock input. Therefore, you should use the logic element (LE) registers in the FPGA to generate the CK and CK# signals. This helps match the CK and CK# signals with the DQ signal and reduces any process, voltage, temperature variations, and skew between CK or CK# and DQ signals.

DM Pins

DDR and DDR2 SDRAM use the data mask (DM) pins during the write operation. Driving the DM pin low indicates that the write is valid. Driving the DM pin high results in the memory masking the DQ signals. You can use any of the I/O pins in the same bank as the DQS/DQ pins to generate the DM signal.

The timing requirements for DM signals at the DDR and DDR2 SDRAM are identical to those of the DQ output signals. Similarly, the DM signals are clocked out by the –90° shifted clock.

Commands & Addresses

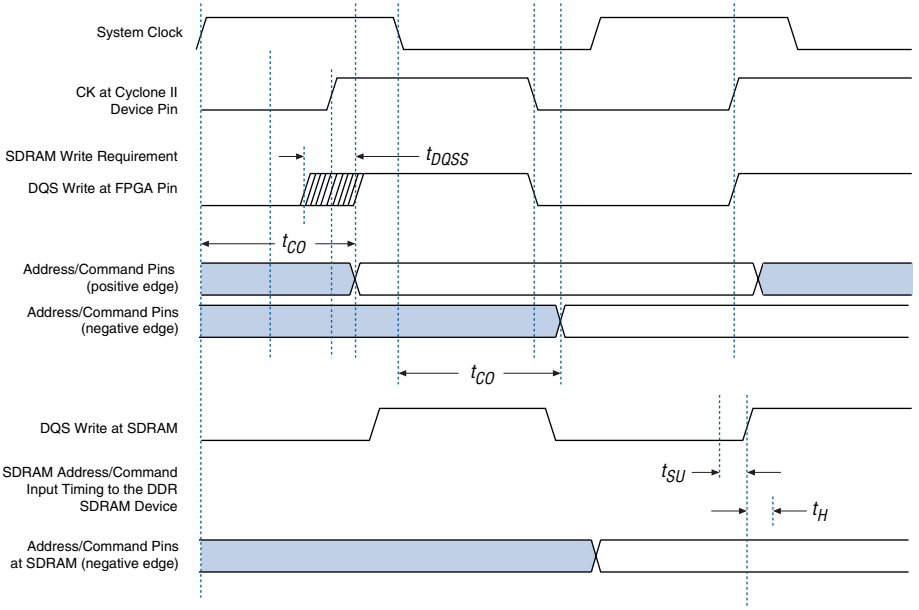
Commands and addresses in DDR and DDR2 SDRAM devices are clocked into the memory using the CK and CK# signals at a single data rate using only the positive clock edge. DDR and DDR2 SDRAM devices have twelve to fourteen address pins, depending on the device capacity. The address pins are multiplexed, so two clock cycles are required to send the row, column, and bank addresses. The CS, RAS, CAS, and WE pins are DDR and DDR2 SDRAM command pins.

The DDR and DDR2 SDRAM address and command inputs both require the same setup and hold times with respect to the DDR and DDR2 SDRAM clocks. The Cyclone II device address and command signals change at the same time as the DQS write signal because they are both generated from the system clock. The positive edge of the DDR and DDR2 SDRAM clocks, CK, is aligned with DQS to satisfy t_{DQSS}. If the command

and address outputs are generated on the clock's positive edge, they may not meet the setup and hold time requirements (see Figure 3 on page 9). Therefore, you should use the negative edge of the system clock for the commands and addresses to the DDR and DDR2 SDRAM. You can use any of the FPGA's I/O pins for the commands and addresses.

Figure 3 shows the address and command timing and the DDR SDRAM t_{DQSS}, t_{DS}, and t_{DH} timing requirements.

Figure 3. Address & Command Timing *Notes (1), (2)*



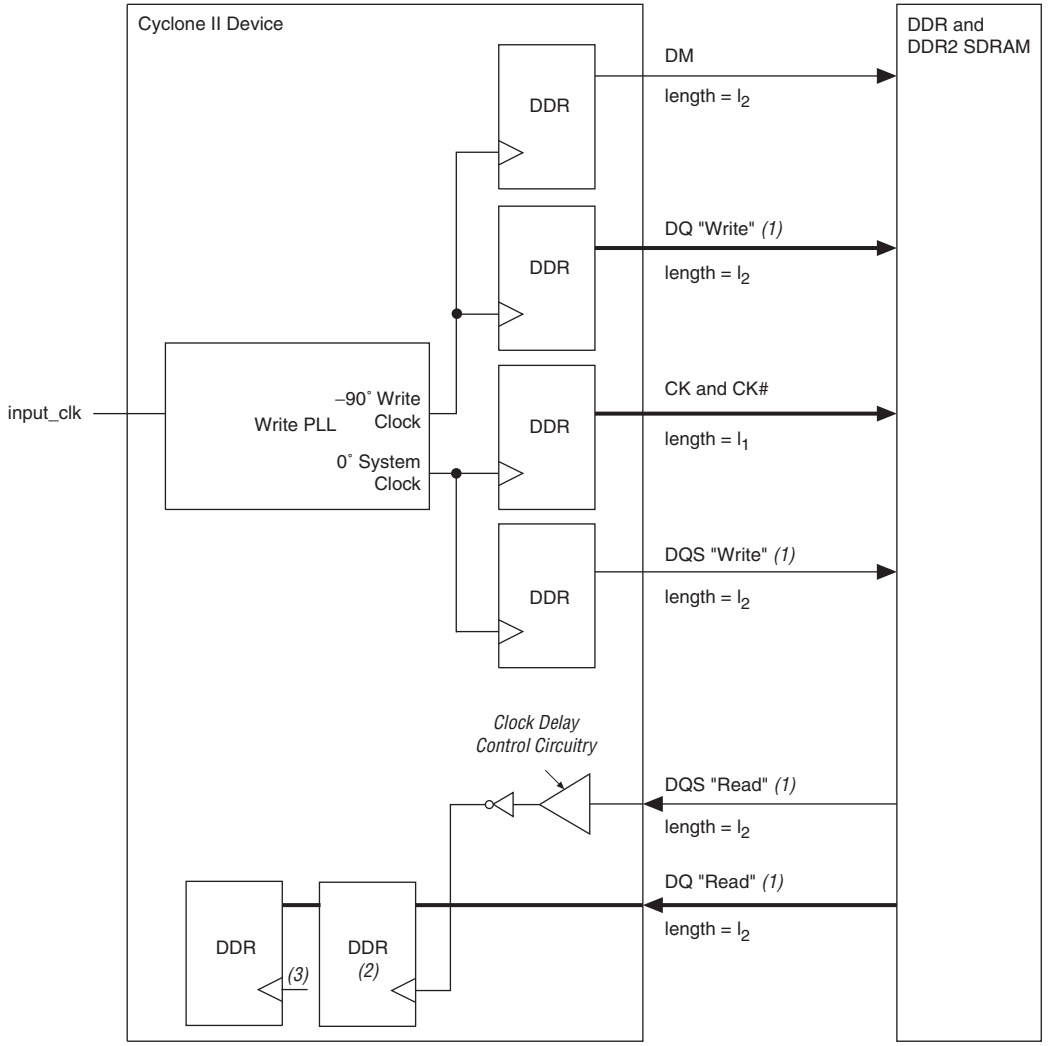
Notes to Figure 3:

(1) The address and command timing shown in Figure 3 is applicable for both reads and writes.

(2) If the board trace lengths for the DQS, CK, address, and command pins are the same, the signal relationships at the Cyclone II device pins are maintained at the DDR and DDR2 SDRAM pins.

Figure 4 shows how the Cyclone II device generates the DQ, DQS, CK, and CK# signals. The write PLL generates the system clock and –90° shifted clock (write clock). The write PLL's input clock can either be the same or a different frequency as the DDR or DDR2 SDRAM frequency of operation. The system clock and write clock have the same frequency as the DQS frequency. The write clock is –90° shifted from the system clock.

Figure 4. DDR & DDR2 SDRAM With Clock Delay Control Circuitry



Notes to Figure 4:

(1) DQ and DQS signals are bidirectional. One DQS signal is associated with a group of DQ signals.

(2) Although there are three LE registers for capturing the read data, this figure only shows one register.

(3) The clock to this register can either be the system clock or another clock output of the write PLL. If the design needs another write PLL clock output, another register is needed to transfer the data back to the system clock domain.

Read Side Implementation Using Clock Delay Control Circuitry

Cyclone II devices have clock delay control circuitry on each DQS pin that allows a delay to center-align the input DQS synchronization signals within the data window of their corresponding DQ data signals at the LE register. This ensures the data is latched at the LE register. The delayed DQS signals drive the global clock network, which in turn clocks the DQ signals on internal LE registers. The DQS signal is inverted before going to the DQ LE clock ports.

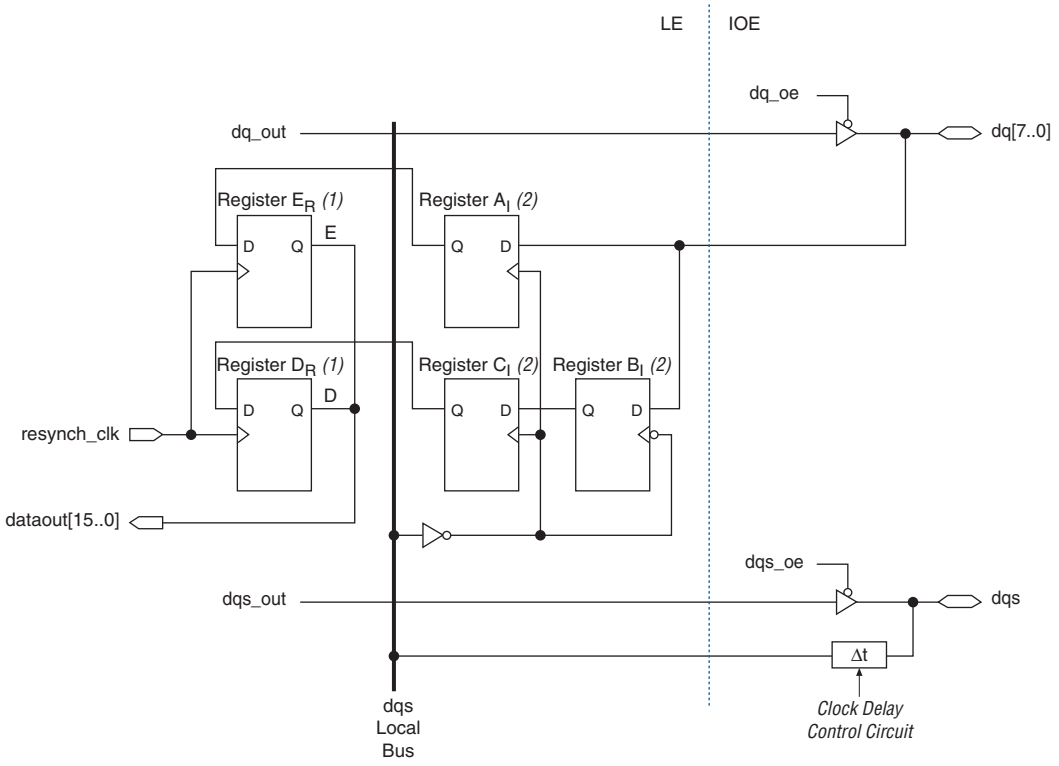
Clock Delay Control Circuitry

The clock delay control circuit is preset to 64 possible delay settings. When a delay time is set, the Quartus® II software chooses the optimum setting from these 64 possible delay settings that results in a delay closest to the delay time assigned. The clock delay control circuit is not compensated for any process, voltage, and temperature (PVT) variations and you should take this into consideration when setting the delay.

See "Read Margin Analysis" on page 16 for more information on how the PVT variation in the clock delay control circuitry affects the design.

Figure 5 shows a more detailed picture of the Cyclone II device read data path for ×8 mode. The DQS signal goes to the clock delay control circuit and is shifted to be center aligned with the incoming data. The shifted DQS signal is then routed to the global clock bus. The DQS global clock bus signal is then inverted before it clocks the DQ at the LE registers. The outputs from the LE input registers then go to the resynchronization registers. The `resynch_clk` signal clocks the resynchronization register. The `resynch_clk` can come from the system clock, the write clock, or the write PLL clock.

Figure 5. DDR & DDR2 SDRAM Read Data Path in Cyclone II Devices



Notes to Figure 5:
(1) Registers E_R and D_R are resynchronization registers.
(2) Registers A_I, B_I, and C_I are capture registers.

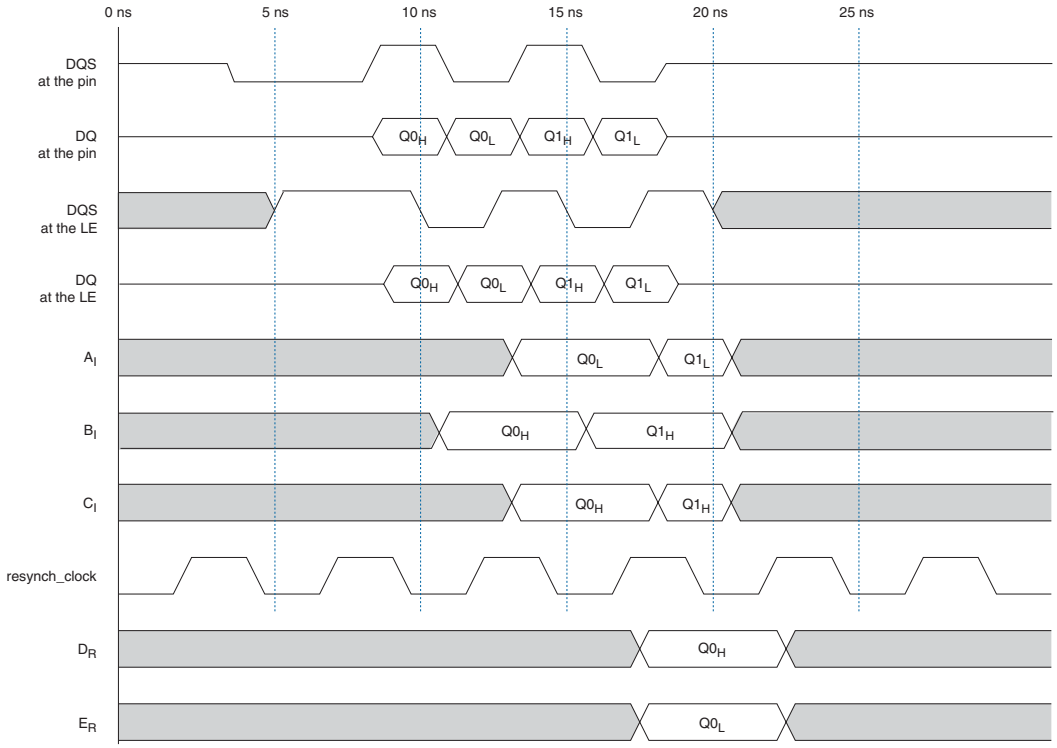
DQS Postamble

The DQ and DQS pins use the SSTL-2 class II I/O standard for DDR SDRAM and the SSTL-18 class II I/O standard for DDR2 SDRAM. When either the Cyclone II or the DDR SDRAM device does not drive the DQ and DQS pins, the signals go to a high-impedance state. Since a pull-up resistor terminates both DQ and DQS to V_{TT} (1.25 V for SSTL-2 and 0.9 V for SSTL-18), the effective voltage on the high-impedance line is 1.25 or 0.9 V, respectively. According to the JEDEC JESD 8-9 specification for the SSTL-2 I/O standard and JEDEC JESD8-15A specification for the SSTL-18 I/O standard, this is an indeterminate logic level and the input buffer can interpret this as either a logic high or logic low. If there is any noise on the DQS line, the input buffer may interpret that noise as actual strobe edges. Therefore, when the DQS signal gets tri-stated after a read postamble, you

should disable the input LE registers so that erroneous data does not get latched in and all the data from the memory gets resynchronized properly.

Figure 6 shows a read operation example when the DQS postamble could be a problem. Figure 6 shows the output waveforms of LE registers A_I, B_I, C_I, D_R, and E_R from Figure 5. Waveform A_I shows the output of register A_I. Waveform B_I shows the output of the LE register B_I. The output of register B_I goes into register C_I whose output is shown in waveform C_I. Waveforms D_R and E_R illustrate the output signals after the resynchronization registers.

Figure 6. Read Example With a DQS Postamble Issue



The first falling edge of the DQS signal at the LE register occurs at 10 ns. At this point, data $Q0_H$ is clocked in by register B_I (waveform B_I). At 12.5 ns, data $Q0_L$ is clocked in by the active high register A_I (waveform A_I) and data $Q0_H$ passes through the register C_I (waveform C_I). In this example, the positive edge of the `resynch_clock` signal occurs at 16.5

ns, where both $Q0_H$ and $Q0_L$ are sampled by the logic element's (LE's) resynchronization registers. Similarly, data $Q1_H$ is clocked in by register B_I at 15 ns, while data $Q1_L$ is clocked in by register A_I and data $Q1_H$ passes through register C_I at 17.5 ns. At 20 ns, assume that noise on the DQS line causes a valid clock edge at the LE registers and changes the values of waveforms A_I, B_I, and C_I. The next rising edge of the `resynch_clock` signal does not occur until 21.5 ns, but data $Q1_L$ and $Q1_H$ are not valid anymore at the output of register A_I and register C_I, so the resynchronization registers do not sample $Q1_L$ and $Q1_H$ and may sample the wrong data instead.

Cyclone II devices have circuitry to prevent false edge trigger at the end of the DQS postamble. Each Cyclone II clock delay control block is connected to a DQS postamble circuit. The DQS postamble circuit is a dynamic enable and disable circuit that, when enabled, allows the global clock bus to be forced low, preventing DQS signal from going to the global clock bus to clock the LE capture registers (see Figure 7). When the memory controller detects the last DQS falling edge, the memory controller must send out a low signal on `ENOUT` to force the global clock bus low. This prevents any glitches from happening right after the postamble. The `ena_register_mode` bit is enabled when the DQS pin is used in DDR mode.

Figure 7. Cyclone II DQS Postamble Circuitry

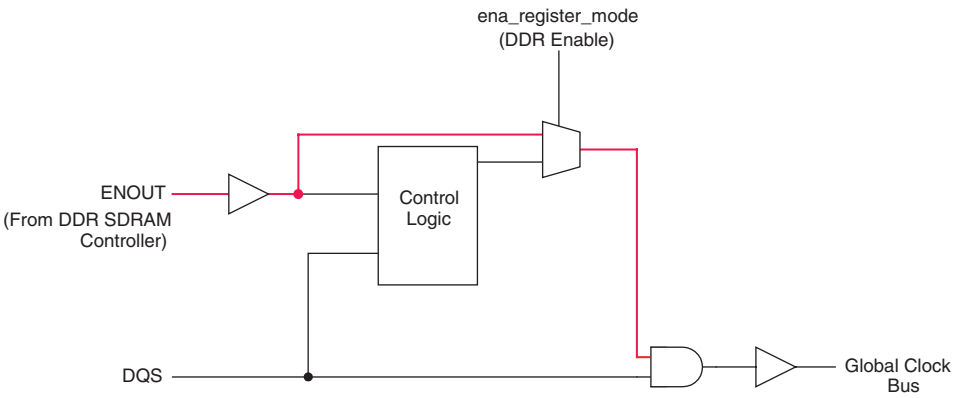


Figure 8 shows the timing waveform for Figure 7. Figure 9 shows the read timing waveform when using the Cyclone II DQS postamble circuit.

Figure 8. Cyclone II DQS Postamble Circuitry Control Timing Waveform

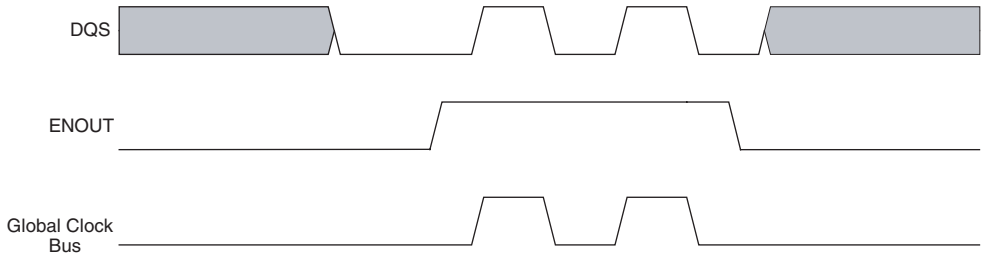
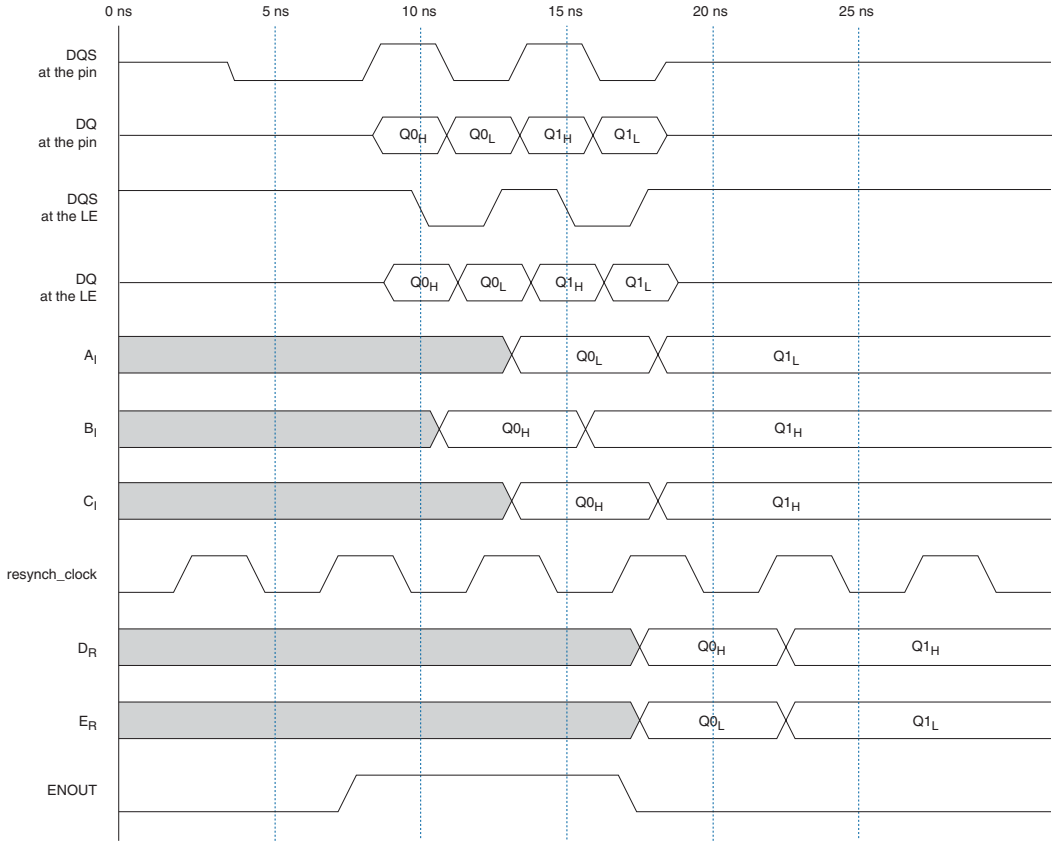


Figure 9. Cyclone II DQS Postamble Circuitry Read Timing Waveform



Read Margin Analysis

Table 5 shows the worst case DDR SDRAM read timing margin analysis at 100, 133, and 167 MHz. Table 6 shows the worst case DDR2 SDRAM read timing margin analysis at 167 MHz. The board trace variation for the DQ and DQS pins is ±50 ps (approximately ±0.3 inches of FR4 trace length

variations). You can perform a similar timing analysis for your interface with other DDR and DDR2 SDRAM memory devices by replacing the t_{HP}, t_{QHS}, and t_{DQSQ} values in Table 4 with those from your memory data sheet.

Table 5. Example Read Timing Analysis for DDR SDRAM When Using Clock Delay Control Circuitry in a -6 Speed Grade EP2C70 Device (Part 1 of 2) *Note (1)*

Parameter	Specification	100 MHz	133 MHz	167 MHz	Description
Memory specifications	t_{HP} *(2)*	4.50 ns	3.38 ns	2.70 ns	Half period as specified by the memory data sheet
	t_{QHS} *(2)*	0.75 ns	0.75 ns	0.50 ns	Data hold skew factor as specified by the memory data sheet
	t_{DQSQ} *(2)*	0.50 ns	0.50 ns	0.40 ns	Skew between DQS and DQ from the memory
	t_{QH} *(2)*	3.75 ns	2.63 ns	2.20 ns	$t_{HP} - t_{QHS}$
FPGA specifications	t_{DC} *(3)*	1.83 ns	1.27 ns	1.01 ns	Ideal clock delay setting
	t_{DCERR}	0.30 ns	0.30 ns	0.30 ns	DQS variations due to PVT variations in the clock delay control circuitry
	t_{DQS2LE_MIN} *(4)*	1.023 ns	1.023 ns	1.023 ns	Minimum DQS pin to LE register delay
	t_{DQS2LE_MAX} *(4)*	2.106 ns	2.106 ns	2.106 ns	Maximum DQS pin to LE register delay
	t_{DQ2LE_MIN} *(4)*	0.874 ns	0.874 ns	0.874 ns	Minimum DQ pin to LE register delay
	t_{DQ2LE_MAX} *(4)*	1.783 ns	1.783 ns	1.783 ns	Maximum DQ pin to LE register delay
	$t_{DQSQINT}$	0.100 ns	0.100 ns	0.100 ns	Internal skew between DQS and DQ inside Cyclone II devices
	μt_{SU}	0.039 ns	0.039 ns	0.039 ns	Intrinsic setup time of the LE register (rounded up)
	μt_{H}	0.153 ns	0.153 ns	0.153 ns	Intrinsic hold time of the LE register (rounded up)
Board specification	t_{EXT}	0.05 ns	0.05 ns	0.05 ns	Board trace variations on the DQ and DQS lines

Table 5. Example Read Timing Analysis for DDR SDRAM When Using Clock Delay Control Circuitry in a -6 Speed Grade EP2C70 Device (Part 2 of 2) *Note (1)*

Parameter	Specification	100 MHz	133 MHz	167 MHz	Description
Timing calculations	t_{SHIFT_MIN}	1.53 ns	0.97 ns	0.71 ns	Minimum shift provided by the clock delay control circuitry ($t_{DC} - t_{DCERR}$)
	t_{SHIFT_MAX}	2.13 ns	1.57 ns	1.31 ns	Maximum shift provided by the clock delay control circuitry ($t_{DC} + t_{DCERR}$)
	t_{DELTA_MIN}	1.679 ns	1.119 ns	0.859 ns	Minimum difference between the DQS and the DQ signal paths ($t_{DQS2LE\_MIN} + t_{SHIFT\_MIN} - t_{DQ2LE\_MIN}$)
	t_{DELTA_MAX}	2.453 ns	1.893 ns	1.633 ns	Maximum difference between the DQS and the DQ signal paths ($t_{DQS2LE\_MAX} + t_{SHIFT\_MAX} - t_{DQ2LE\_MAX}$)
Results	Read setup timing margin	0.99 ns	0.43 ns	0.27 ns	$t_{DELTA\_MIN} - t_{DQSQ} - t_{EXT} - t_{DQSQINT} - \mu t_{SU}$
	Read hold timing margin	0.994 ns	0.434 ns	0.264 ns	$t_{QH} - \mu t_{H} - t_{EXT} - t_{DQSQINT} - t_{DELTA\_MAX}$

Notes to Table 5:

(1) These numbers are preliminary until Cyclone II characterization is final.
(2) The memory numbers used here come from Micron MT46V16M8TG/MT46V8M16TG devices. The -75 speed grade is used for 100 and 133 MHz. The -6 speed grade is used for 167 MHz.
(3) This timing calculation is based on equal setup and hold slack.
(4) These numbers are from the Quartus II software, version 4.1 Service Pack 1. Altera recommends using the latest version of the Quartus II software for your design.

Table 6. Example Read Timing Analysis for DDR2 SDRAM When Using Clock Delay Control Circuitry in a -6 Speed Grade EP2C70 Device (Part 1 of 2) *Note (1)*

Parameter	Specification	167 MHz	Description
Memory specifications	t_{HP} *(2)*	2.70 ns	Half period as specified by the memory data sheet
	t_{QHS} *(2)*	0.45 ns	Data hold skew factor as specified by the memory data sheet
	t_{DQSQ} *(2)*	0.35 ns	Skew between DQS and DQ from the memory
	t_{QH} *(2)*	2.25 ns	$t_{HP} - t_{QHS}$

Table 6. Example Read Timing Analysis for DDR2 SDRAM When Using Clock Delay Control Circuitry in a -6 Speed Grade EP2C70 Device (Part 2 of 2) Note (1)

Parameter	Specification	167 MHz	Description
FPGA specifications	t_{DC} (3)	1.01 ns	Ideal clock delay setting
	t_{DCERR}	0.3 ns	DQS variations due to PVT variation in the clock delay control circuitry
	t_{DQS2LE_MIN} (4)	1.041 ns	Minimum DQS pin to LE register delay
	t_{DQS2LE_MAX} (4)	2.141 ns	Maximum DQS pin to LE register delay
	t_{DQ2LE_MIN} (4)	0.892 ns	Minimum DQ pin to LE register delay
	t_{DQ2LE_MAX} (4)	1.818 ns	Maximum DQ pin to LE register delay
	$t_{DQSQINT}$	0.100 ns	Internal skew between DQS and DQ inside Cyclone II devices
	μt_{SU}	0.039 ns	Intrinsic setup time of the LE register (rounded up)
	μt_{H}	0.153 ns	Intrinsic hold time of the LE register (rounded up)
Board specification	t_{EXT}	0.05 ns	Board trace variations on the DQ and DQS lines
Timing calculations	t_{SHIFT_MIN}	0.71 ns	Minimum shift provided by the clock delay control circuitry ($t_{DC} - t_{DCERR}$)
	t_{SHIFT_MAX}	1.31 ns	Maximum shift provided by the clock delay control circuitry ($t_{DC} + t_{DCERR}$)
	t_{DELTA_MIN}	0.859 ns	Minimum difference between the DQS and the DQ signal paths ($t_{DQS2LE\_MIN} + t_{SHIFT\_MIN} - t_{DQ2LE\_MIN}$)
	t_{DELTA_MAX}	1.633 ns	Maximum difference between the DQS and the DQ signal paths ($t_{DQS2LE\_MAX} + t_{SHIFT\_MAX} - t_{DQ2LE\_MAX}$)
Results	Read setup timing margin	0.32 ns	$t_{DELTA\_MIN} - t_{DQSQ} - t_{EXT} - t_{DQSQINT} - \mu t_{SU}$
	Read hold timing margin	0.314 ns	$t_{QH} - \mu t_{H} - t_{EXT} - t_{DQSQINT} - t_{DELTA\_MAX}$

Notes to Table 6:

(1) These numbers are preliminary until Cyclone II characterization is final.

(2) The memory numbers used here come from Micron MT47H64M4-16/MT47H32M8-8/MT47H16M16-4 devices. The -5 speed grade is used for 167 MHz.

(3) This timing calculation is based on equal setup and hold slack.

(4) These numbers are from the Quartus II software, version 4.1 Service Pack 1. Altera recommends using the latest version of the Quartus II software for your design.

In order to achieve the optimum sampling window, calculate the amount of delay for the DQS signal (t_{DC}). To account for the PVT variation of the programmable delay chain, add t_{DCERR} to t_{DC} as shown in the following equations.

$$t_{SHIFT}(\text{maximum}) = t_{DC} + t_{DCERR}$$

$$t_{SHIFT}(\text{minimum}) = t_{DC} - t_{DCERR}$$

Table 7 shows the DQS and DQ path delays to the LE registers when the clock delay control is set to zero delay and the I/O standard is set to SSTL-2 class II.

Table 7. DQS & DQ Internal Delay Using SSTL-2 *Notes (1), (2)*

Specification	-6 Speed Grade Commercial Device	-7 Speed Grade Commercial Device	-8 Speed Grade Commercial Device	Description
t_{DQS2LE}(minimum)	1.023 ns	1.023 ns	1.023 ns	Minimum internal delay from DQS pad to LE register
t_{DQS2LE}(maximum)	2.106 ns	2.417 ns	2.734 ns	Maximum internal delay from DQS pad to LE register
t_{DQ2LE}(minimum)	0.874 ns	0.874 ns	0.874 ns	Minimum internal delay from DQ pad to LE register
t_{DQ2LE}(maximum)	1.783 ns	2.048 ns	2.315 ns	Maximum internal delay from DQ pad to LE register

Notes to Table 7:
(1) These numbers are preliminary until Cyclone II timing models are final.
(2) These numbers are from the Quartus II software, version 4.1 Service Pack 1. Altera recommends using the latest version of the Quartus II software for your design.

Table 8 shows the DQS and DQ path delays to the LE registers when the clock delay control is set to zero delay and the I/O standard is set to SSTL-18 class II.

Table 8. DQS & DQ Internal Delay Using SSTL-18 *Note (1), (2)*

Specification	-6 Speed Grade Commercial Device	-7 Speed Grade Commercial Device	Description
t_{DQS2LE}(minimum)	1.041 ns	1.041 ns	Minimum internal delay from DQS pad to LE register
t_{DQS2LE}(maximum)	2.141 ns	2.458 ns	Maximum internal delay from DQS pad to LE register
t_{DQ2LE}(minimum)	0.892 ns	0.892 ns	Minimum internal delay from DQ pad to LE register
t_{DQ2LE}(maximum)	1.818 ns	2.089 ns	Maximum internal delay from DQ pad to LE register

Notes to Table 8:

(1) These numbers are preliminary until Cyclone II timing models are final.

(2) These numbers are from the Quartus II software, version 4.1 Service Pack 1. Altera recommends using the latest version of the Quartus II software for your design.

From Figure 10 on page 22, the setup slack is:

$$\text{Setup slack} = \text{minimum DQS shift} - \text{minimum DQ shift} - \mu t_{SU}$$
$$= [t_{SHIFT}(\text{minimum}) + t_{DQS2LE}(\text{minimum})] - [t_{DQ2LE}(\text{minimum}) + t_{DQSQ} + t_{EXT} + t_{DQSQINT}] - \mu t_{SU}$$

Similarly, the hold slack is:

$$\text{Hold slack} = \text{maximum DQ shift} - \text{maximum DQS shift} - \mu t_{H}$$
$$= [t_{DV\_MEM} + t_{DQ2LE}(\text{maximum}) + t_{DQSQ} - t_{EXT} - t_{DQSQINT}] - [t_{SHIFT}(\text{maximum}) + t_{DQS2LE}(\text{maximum})] - \mu t_{H}$$
$$= [t_{QH} + t_{DQ2LE}(\text{maximum}) - t_{EXT} - t_{DQSQINT}] - [t_{SHIFT}(\text{maximum}) + t_{DQS2LE}(\text{maximum})] - \mu t_{H}$$

If the setup slack equals the hold slack, you can find the optimum amount of DQS delay needed to achieve even setup and hold slack.

$$t_{DC} = 0.5 \times \{t_{QH} + t_{DQSQ} + \mu t_{SU} - \mu t_{H} + [t_{DQ2LE}(\text{maximum}) + t_{DQ2LE}(\text{minimum})] - [t_{DQS2LE}(\text{maximum}) + t_{DQS2LE}(\text{minimum})]\}$$

Using the results from Tables 4 and 5 for the 167-MHz DDR SDRAM memory:

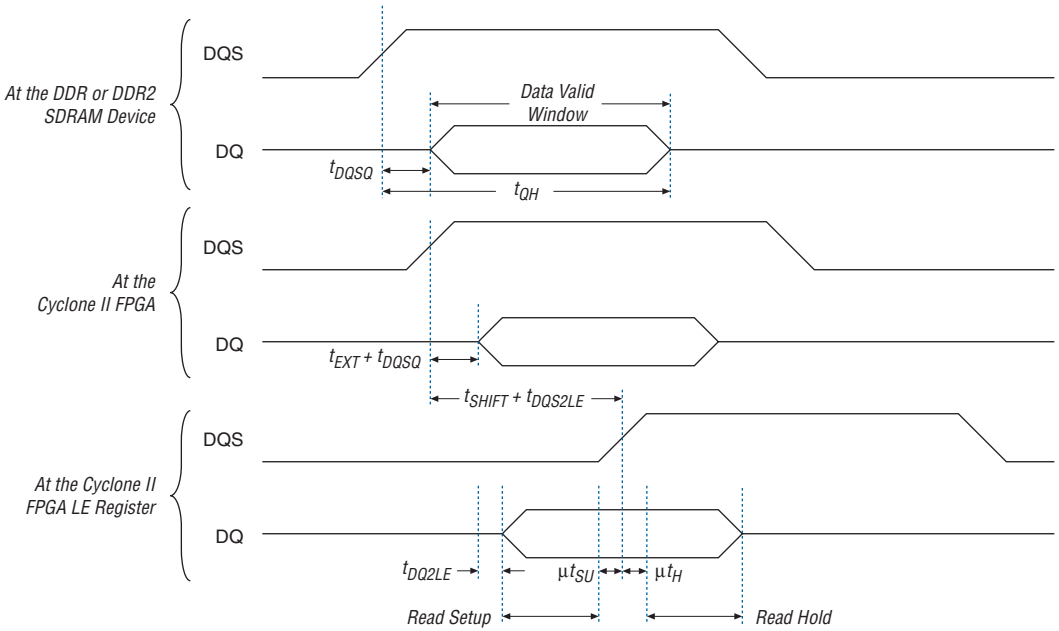
$t_{DC} = 0.5 \times \{2.2 + 0.4 + 0.039 - 0.153 + [1.783 + 0.874] - [2.106 + 1.023]\}$
$= 1.01$ ns

Therefore, the optimum delay needed for 167-MHz DDR SDRAM is:

Phase shift = $(1.01/6) \times 360° = 60°$

The delay required to center DQS within DQ is not exactly 90°.

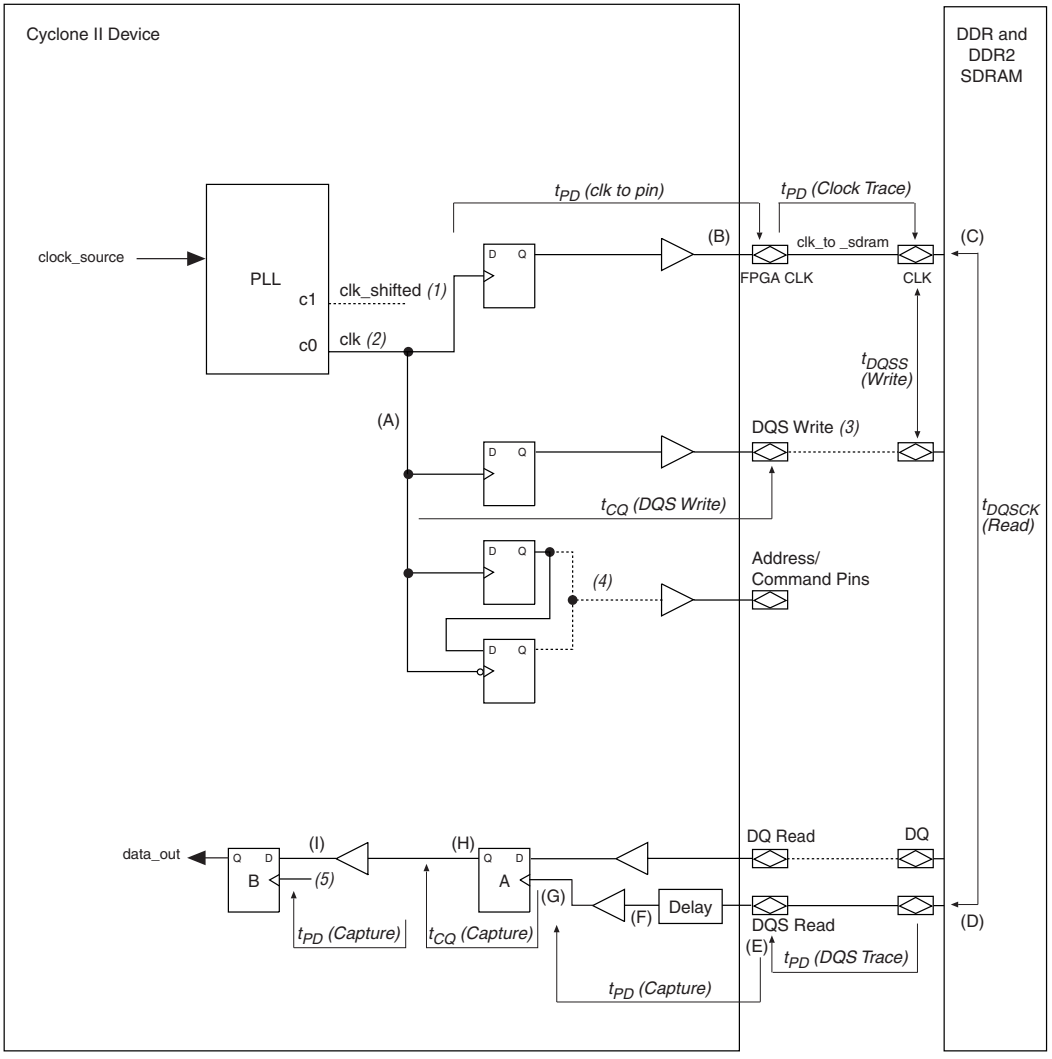
Figure 10. DQS & DQ Signals During a Read



Round Trip Delay

Figure 11 shows the timing analysis and illustration of the round trip delay. The round trip delay is the delay from the FPGA clock to the DDR or DDR2 SDRAM and back to the FPGA (input to register B). The analysis is required to reliably transfer data from the register A, which is in the DQS clock domain, to register B, which is in the system clock domain.

Figure 11. Round Trip Delay



Notes to Figure 11:

(1) The `clk_shifted` signal is shown for completeness, but it is not needed in the timing analysis for round-trip delay or address or command timing.

(2) `clk` is the system clock.

(3) The DQS signal is bidirectional. DQS write and DQS read are shown as two separate pins for this timing analysis.

(4) You can clock the address/command register with either a rising or falling edge of the system clock signal.

(5) You can use `clk`, `clk_shifted`, or `resynch_clk` as the clock input for register B. The `clk` and `clk_shifted` signals can also be inverted at register B if necessary.

Register A in Figure 11 represent the DDR capture logic. The Q output from register A represents the point at which the read data is converted from DDR to SDR. At the output of register A, the data is already at single data rate, but is still in the DQS clock domain. Q_H (DQ data during DQS high) is sampled on the positive edge of the 90° phase-shifted DQS pulse, but re-sampled on the negative edge of the 90° phase-shifted DQS pulse, to align it with Q_L (DQ data during DQS low).

Once sampled by the negative edge of the 90° phase-shifted DQS pulse, Q_L and Q_H are available for resynchronization.

To sample the Q output of register A into register B, you need the time relationship between register B's clock input and the D input, which depends on the phase relationship between DQS and the clock signal and involves the following steps:

1. Calculate the system's round trip delay.
2. Select a resynchronization phase of the system clock or other available clock that reliably samples the Q output of register A, based on the calculated safe resynchronization window. See Figure 12.
3. Apply the correct clock edge for your resynchronization logic in your memory controller.

You can use the `clk` or `clk_shifted` signals as the register B clock input. You can invert `clk` and `clk_shifted` if needed. To determine the timing of data at the D input of register B relative to `clk`, consider the following timing-path dependencies, which are in chronological order:

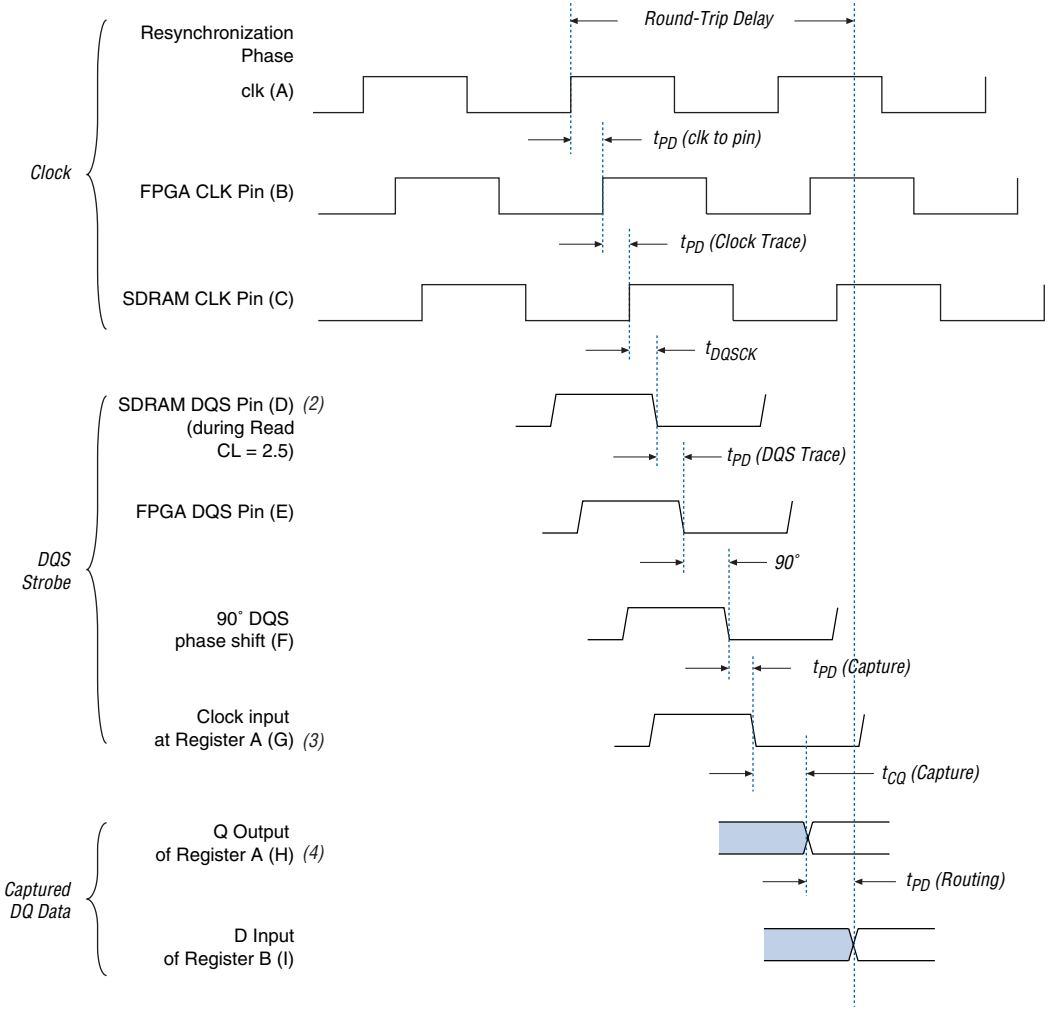
- The DDR/DDR2 SDRAM clock input arrives (a delayed version of `clk`)
- DQS strobe from the DDR/DDR2 SDRAM arrives at the clock input of register A
- Data arrives at the Q output of register A
- Data arrives at the D input of register B

There are three main parts to this path:

- Clock delays between the FPGA global clock net and the DDR or DDR2 SDRAM clock input
- DQS strobe delays between the DDR or DDR2 SDRAM clock input and DQS's arrival at the FPGA capture registers
- Read data delays between the output of register A and the input of register B

Figure 11 shows the individual delays between points (A) and (K). The sum of all these delays is the round trip delay. Figure 12 shows the timing relationship of the signals for the delays between points (A) to (I) for a DDR SDRAM of CAS latency of 2.5.

Figure 12. RTD Calculation for DDR SDRAM



To determine the point at which the data can be reliably resynchronized, calculate the minimum and maximum round-trip delay. You can then determine what resynchronization logic to use for your system. Make sure to take PVT variations into account.

Delay (A) to (B) is the clock-to-output time to generate the clock signals to the DDR or DDR2 SDRAM device.

Delay (B) to (C) is the trace delay for the clock. If there are multiple devices in the system, use the one furthest away from the FPGA for the maximum calculation and the one closest to the FPGA for the minimum calculation.

Delay (C) to (D) is the relationship between the clock and the DQS strobe timing during reads. The t_{DQSCK} time in DDR and DDR2 SDRAM specifications is nominally 0, but varies by ±0.75 ns for DDR SDRAM and ±0.5 ns for DDR2 SDRAM, depending the device speed grade. The DQS output strobe is guaranteed to be within $\pm t_{DQSCK}$ of the clock input. Use t_{DQSCK}(maximum), typically +0.75 ns for DDR SDRAM and +0.5 ns for DDR2 SDRAM, to calculate the maximum round-trip delay and use t_{DQSCK}(minimum), typically –0.75 ns for DDR SDRAM and –0.5 ns for DDR2 SDRAM, to calculate the minimum delay.

Delay (D) to (E) is the trace delay for DQS, which typically matches the trace delay for the DQ signals in the same byte group. To calculate the maximum round-trip delay, use the byte group with the longest trace lengths. Use the byte group with the shortest trace lengths to calculate the minimum round-trip delay. Similarly, if there are multiple devices in the system, use the one furthest from the FPGA for the maximum calculation and the one closest to the FPGA for the minimum. Trace lengths between different byte groups do not have to be tightly matched, but a difference between the longest and shortest trace lengths decreases the safe resynchronization window, the window size within which the data can be reliably resynchronized.

To calculate the maximum round trip delay, use the longest delay for the whole interface and use the shortest delay for the whole interface for the minimum round trip delay.

PLL jitter, clock duty cycle, and the half cycle used to align Q_H and Q_L also affect the round-trip delay. You must add each of these delays to the maximum round-trip delay and subtract them from the minimum round-trip delay.

Write Side Implementation

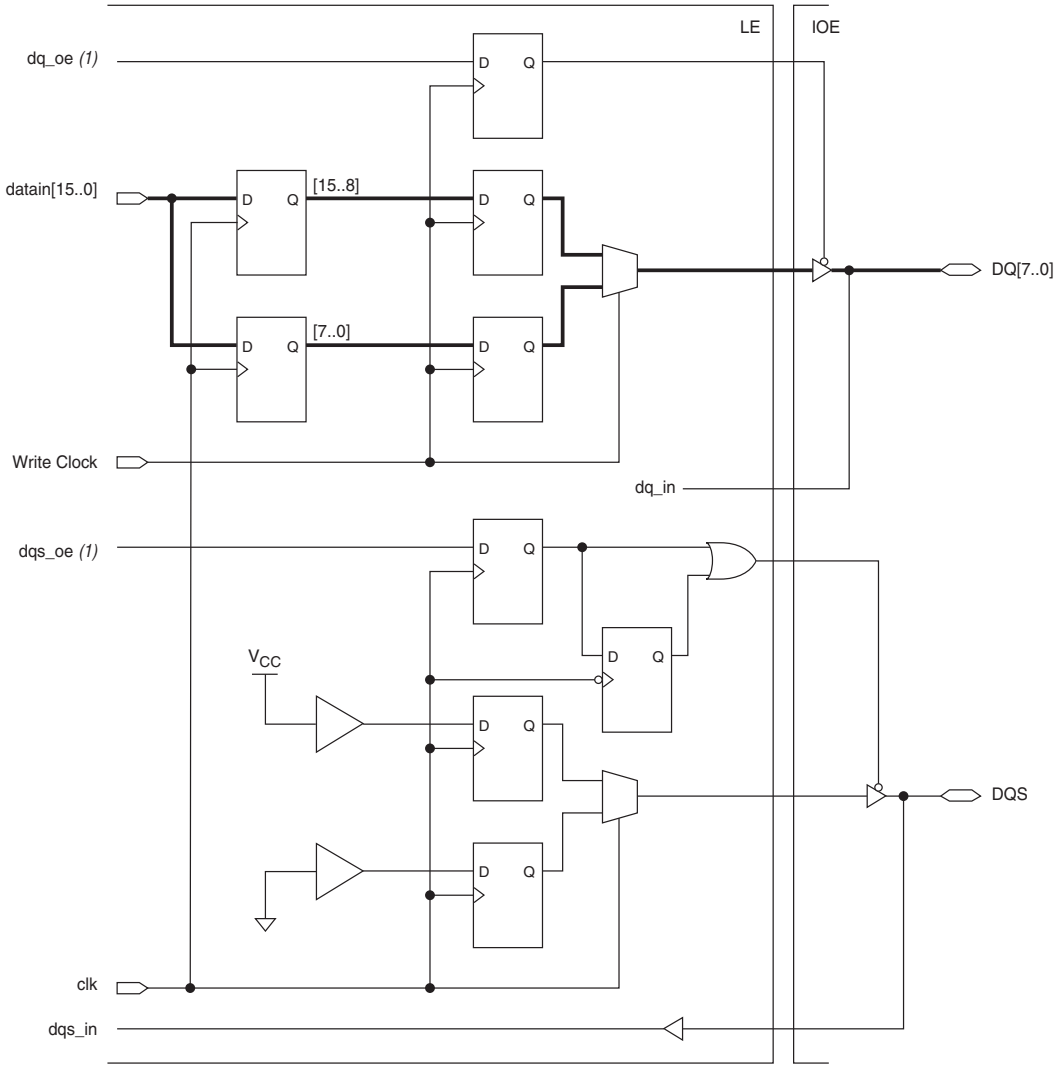
Altera recommends one implementation for the write operation (see Figure 4 on page 10) where the write side uses a PLL to generate the clocks listed in Table 9.

Table 9. Write Side PLL Clocks

Clock	Description
System clock	This is used for the memory controller and to generate the DQS write and CK/CK# signals.
Write clock (–90° shifted from system clock)	This is used in the data path to generate the DQ write signals.

Figure 13 shows the data path for DDR and DDR2 SDRAM write operations.

Figure 13. Cyclone II DDR & DDR2 SDRAM Write Data Path



Writing Timing Margin Analysis

Table 10 shows the DDR SDRAM write timing margin analysis at 100, 133, and 167 MHz. Table 11 shows the DDR2 SDRAM write timing margin analysis at 167 MHz, when the board trace variations for the DQ and DQS pins is ±50 ps (approximately ±0.3 inches of FR4 trace length

variations). You can perform a similar timing analysis for your interface with a different type of DDR and DDR2 SDRAM memory. You only need the t_{DS} and t_{DH} values from the memory data sheet.

Table 10. Write Timing Analysis for DDR SDRAM Using an -6 Speed Grade EP2C70 Device *Note (1)*

Parameter	Specification	100 MHz	133 MHz	167 MHz	Description
Memory specifications	t_{CK}	10.0 ns	7.5 ns	6.0 ns	Clock period
	$t_{DS} = t_{DH}$ *(2)*	0.50 ns	0.50 ns	0.45 ns	DQ and DM setup and hold time from the memory data sheet
FPGA specifications	t_{IOSKEW}	0.10 ns	0.10 ns	0.10 ns	DQS-DQ skew from the FPGA
	$t_{CLKSKEW}$	±0.15 ns	±0.15 ns	±0.15 ns	Skew between two PLL outputs
	t_{DCD}	0.50 ns	0.38 ns	0.30 ns	Duty cycle distortion (5% of clock period)
Board specifications	t_{EXT}	±0.05 ns	±0.05 ns	±0.05 ns	Board trace variations on the DQ and DQS lines (167 ps per inch for an FR4 trace)
Timing calculations	t_{SHIFT_MIN}	2.35 ns	1.725 ns	1.35 ns	Minimum shift from the PLL ($0.25 \times t_{CK}$ (90° shift) – $t_{CLKSKEW}$)
	t_{SHIFT_MAX}	2.65 ns	2.025 ns	1.65 ns	Maximum shift from the PLL ($0.25 \times t_{CK}$ (90° shift) + $t_{CLKSKEW}$)
Results	Write setup timing margin	1.20 ns	0.70 ns	0.45 ns	$t_{SHIFT\_MIN} - t_{DCD} - t_{IOSKEW} - t_{EXT} - t_{DS}$
	Write hold timing margin	1.20 ns	0.70 ns	0.45 ns	$0.5 \times t_{CK} - t_{SHIFT\_MAX} - t_{DCD} - t_{IOSKEW} - t_{EXT} - t_{DH}$

Notes to Table 10:

(1) These numbers are preliminary until Cyclone II device characterization is complete.

(2) These memory numbers come from Micron MT46V16M8TG/MT46V8M16TG devices. The -75 speed grade is used for 100 and 133 MHz. The -6 speed grade is used for 167 MHz.

Table 11. Write Timing Analysis for DDR2 SDRAM Using an -6 Speed Grade EP2C70 Device *Note (1)*

Parameter	Specification	167 MHz	Description
Memory specifications	t_{CK}	6.0 ns	Clock period
	t_{DS} *(2)*	0.15 ns	DQ and DM setup time from the memory data sheet
	t_{DH} *(2)*	0.28 ns	DQ and DM hold time from the memory data sheet
FPGA specifications	t_{IOSKEW}	0.10 ns	DQS-DQ skew from Cyclone II devices
	$t_{CLKSKEW}$	±0.15 ns	Skew between two PLL outputs
	t_{DCD}	0.30 ns	Duty cycle distortion (5% of clock period)
Board specifications	t_{EXT}	±0.05 ns	Board trace variations on the DQ and DQS lines (167 ps per inch for an FR4 trace)
Timing calculations	t_{SHIFT_MIN}	1.35 ns	Minimum shift from the PLL ($0.25 \times t_{CK}$ (90° shift) – $t_{CLKSKEW}$)
	t_{SHIFT_MAX}	1.65 ns	Maximum shift from the PLL ($0.25 \times t_{CK}$ (90° shift) + $t_{CLKSKEW}$)
Results	Write setup timing margin	0.75 ns	$t_{SHIFT\_MIN} - t_{DCD} - t_{IOSKEW} - t_{EXT} - t_{DS}$
	Write hold timing margin	0.62 ns	$0.5 \times t_{CK} - t_{SHIFT\_MAX} - t_{DCD} - t_{IOSKEW} - t_{EXT} - t_{DH}$

Notes to Table 11:

(1) These numbers are preliminary until Cyclone II device characterization is complete.

(2) The memory numbers used here come from Micron MT47H64M4-16/MT47H32M8-8/MT47H16M16-4 devices. The -5 speed grade is used for 167 MHz.

Conclusion

DDR and DDR2 SDRAM devices are widely used in FPGA designs, and the DDR technology is the most popular DRAM architecture. Cyclone II devices have dedicated circuitry to interface with DDR and DDR2 SDRAM at speeds up to 167 MHz with comfortable and consistent margins. Additionally, this allows system designers to enhance their Cyclone II system performance through the use of commercial off the shelf PC memory, reducing cost. The Cyclone II device's DDR and DDR2 interface allows designers to use these devices in applications that require fast data transmission, simplified the system design, and improved performance.

References

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JEDEC Standard Publication JESD8-9B, Stub Series Termination Logic for 2.5V (SSTL-2), JEDEC Solid State Technology Association.

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MT46V16M8TG/MT46V8M16TG, 128Mb: x8, x16 DDR SDRAM Data Sheet, Micron Technology, Inc.

MT47H64M4/MT47H32M8/MT47H16M16, 256Mb: x4, x8, x16 DDR2 SDRAM Data Sheet, Micron Technology, Inc.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com